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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/020,586	10/29/2001	Andrew Cox	915.395	5687	
4955	7590 10/19/2004		EXAMI	NER	
WARE FRESSOLA VAN DER SLUYS &			CHAWAN, S	CHAWAN, SHEELA C	
ADOLPHSON, LLP BRADFORD GREEN BUILDING 5 755 MAIN STREET, P O BOX 224 MONROE, CT 06468			ART UNIT	PAPER NUMBER	
			2625	4	
			DATE MAILED: 10/19/2004	· T	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)		
•	10/020,586	COX, ANDREW		
Office Action Summary	Examiner	Art Unit		
•	Sheela C Chawan	2625		
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply				
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period w - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be timy within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).		
Status				
Responsive to communication(s) filed on <u>29 October 2001</u> . 2a) This action is FINAL . 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.				
Disposition of Claims				
4) ☐ Claim(s) 1-23 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-23 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and/or	vn from consideration.			
Application Papers				
 9) The specification is objected to by the Examine 10) The drawing(s) filed on 29 October 2001 is/are: Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Ex 	a)⊠ accepted or b)⊡ objected drawing(s) be held in abeyance. See ion is required if the drawing(s) is ob	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).		
Priority under 35 U.S.C. § 119				
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) □ All b) □ Some * c) ☒ None of: 1. ☒ Certified copies of the priority documents have been received. 2. □ Certified copies of the priority documents have been received in Application No 3. □ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 				
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:			

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DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in United Kingdom on 11/01/00. It is noted, however, that applicant has not filed a certified copy of the 0026726.0 application as required by 35 U.S.C. 119(b).

Preliminary Amendment

2. Preliminary amendment filed on 10/29/01has been entered.

Drawings

3. The Examiner has approved drawings filed on 10/29/01.

Claim Rejections - 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1- 7, 9 -19, 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Maeda et al., (US. 5,309,108).

As to claim 1, Maeda discloses a method of testing functionality of an image display device (testing and detecting a defects on a display which consist of a thin film transistor liquid crystal substrate corresponds to display device, (column 1, lines 10-13 fig 5, element 30) that comprises a matrix (fig 1; 2, 3 and 4(a), corresponds to display matrix, column 1, lines 14- 17, matrix corresponds to a thin film transistor liquid crystal

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the arrangement of matrix consist of 5x5 pixel which comprises of scan lines fig 1, element 11-15 and signal lines fig 1, elements 21-25) of image elements that are individually energisable in a graphical display, the method comprising capturing data corresponding to first (image under voltage application corresponds to first image), and second images (image before voltage application corresponds to a second image) of the display- provided by the device under different test condition thereof, and utilizing the image data for the first and second images to identify a malfunction of the device (in fig 9, subtracted image identifies the malfunction of the device, column 4, lines 36-62, column 12, lines 13-42).

As to claims 2 and 14, Maeda discloses a method including energizing (image under voltage application corresponds to first image) and de-energising images to the elements individually to produce the data corresponding to the first and second images such that elements energized for the first image data capture are de-energized for capturing the second image data (fig 9, column 16, lines 17-64. As depicted in fig 9, elements that are energized for the image under voltage application are de-energized for image before voltage application).

As to claims 3 and 15, Maeda discloses a method including capturing data corresponding to the first image when all of the image elements are energized, image under voltage application corresponds to first image (image under voltage application corresponds to first image, fig 9, column 10, lines 30-65) and capturing data corresponding to the second image when none of the image elements are energized (image before voltage application corresponds to a second image).

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As per claims 4 and 16, Maeda discloses a method including capturing data corresponding to the first and second images when alternate ones of the matrix of image elements are energized and de-energized and such that elements energized for the first image data capture are de-energized for capturing the second image data (column 15, lines 15-19, rows and columns of matrix are energised for first image under voltage application) and de-energized for second image (image before voltage application).

As per claims 5 and 17, Maeda discloses a method wherein utilizing of the image data includes comparing the image data for the first and second images to derive resultant data (column 6, lines 30- 45), corresponding to the functionality of the elements individually (column 7, lines 36-51, column 16, lines 17-29).

As to claims 6 and 18, Maeda discloses a method wherein the elements are configured in an array of rows and columns (matrix corresponds to a thin film transistor liquid crystal, the arrangement of matrix consist of 5x5 pixel which comprises of scan lines fig 1, element 11-15 and signal lines fig 1, elements 21-25), and including combining the resultant data for at least a part an individual one of the rows or columns (column 16, lines 17-39), and comparing the combined (note, fig 9, shows the resultant image by comparing the image under voltage and image before voltage application) data with a threshold (column 17, lines 6-15) to provide an indication of a malfunction in the device (fig 12, column 12, lines 56-64).

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As to claims 7 and 19, Maeda discloses method wherein the value of the threshold is determined as a function of the resultant data (column 6, lines 30-45, column 16, lines 22-39).

As to claims 9 and 21, Maeda discloses a method including capturing the image data with an electronic camera (fig 5, element 48 a detector corresponds to electronic camera, column 11, lines 60 – 65).

As to claim 10, Maeda discloses a method wherein the display device comprises a liquid crystal display device (fig 5, element 30, corresponds to thin film transistor liquid crystal substrate, column 11, lines 58-65).

As to claim 11, Maeda discloses a method wherein the display device (fig 5, element 30 corresponds to thin film transistor liquid crystal substrate, column 11, lines 58-65) is mounted in an electronic apparatus (fig 5, element 48, a detector corresponds to electronic camera, column 11, lines 60 – 65) with a back light operable to illuminate the display device (fig 5, element 105, transmission illumination corresponds to back light illuminating device, column 11, lines 25-32, 49-65), including capturing (fig 5, element 106, a visible image detection processing system corresponds to capturing image, column 11, lines 25-31, 56-65) the data corresponding to the first (fig 9, image under voltage application corresponds to first image) and second images (fig 9, image before voltage application corresponds to a second image) with the back light in use (fig 5, element 105, transmission illumination corresponds to back light illuminating device, column 11, lines 25-32, 49-65).

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As to claim 12, claim 12 recites similar limitation as claim 1 above and similarly analyzed. Maeda teaches the apparatus comprising an optical image capture device configured to capture data (fig 5, element 102, corresponds to optical image, column 11, lines 25-65).

As per claim 13, Maeda discloses apparatus according to a test pattern generator configured to provide first and second electrical test patterns for energising the matrix of image elements to produce said first and second images (column 9, lines 62-68, fig 9, column 13, lines 26-34).

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 20, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al., (US. 5,309,108), as applied to claims 1-7,9-19,21 above and further in view Hawthorne et al., (US.5, 917,935).

Regarding claims 8 and 20, Maeda discloses a method and an apparatus for inspecting a thin film transistor liquid crystal substrate used for a liquid crystal display apparatus, as a pattern to be inspected. Maeda is silent about specific details wherein

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the threshold is a weighted combination of the mean and standard deviation of the values of the resultant data included within the individual row or column.

Hawthorne discloses method and apparatus for automatic test inspection and classifying defects for detection of Mura type defects in substrates. Substrates include liquid crystal flat panel displays, active matrix displays. The system comprises of:

wherein the threshold is a weighted combination of the mean and standard deviation (column 12, lines 37-41, column 13, lines 11-14, 40-59) of the values of the resultant data included within the individual row or column (column 17, lines 39 – 42).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Maeda to include the threshold that is weighted combination of the mean and standard deviation of the values of the resultant data included within the individual row or column. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Maeda by the teaching of Hawthorne to determine a threshold value for each enhanced image determined in response to the mean and standard deviation for the entire respective enhanced image in order to efficiently identify, and classify defects such as mura defects and the like are often desirable (as suggested by Hawthorne column 2, lines 5-7, column 12, lines 37-47).

Regarding claim 22, Maeda discloses an image data for the first (image under voltage application corresponds to first image) and second images (image before voltage application corresponds to a second image) to be compared so as to identify a malfunction of the device (in fig 9, subtracted image identifies the malfunction of the

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device, column 4, lines 36-62, column 12, lines 13-42). Maeda is silent about a computer program to be run on processor. However, Hawthorne discloses a computer system including a computer program for detecting Mura defects in a substrate for a liquid crystal display program to be run on processor (column 3, lines 1-14, column 6, lines 29-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Maeda to include a computer program for detecting defects in a substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Maeda by the teaching of Hawthorne in which an image of the substrate previously acquired may be retrieved from computer memory using computer program, (as suggested by Hawthorne at column 9, lines 45-47).

As to claim 23, Maeda discloses a processor to compare the image data for the first (image under voltage application corresponds to first image) and second (image before voltage application corresponds to a second image) images so as to provide resultant data corresponding to malfunctions occurring individually in an array of regions of the device configured in rows and columns (matrix corresponds to a thin film transistor liquid crystal, the arrangement of matrix consist of 5x5 pixel which comprises of scan lines fig 1, element 11-15 and signal lines fig 1, elements 21-25), to combine the resultant data for at least part of an individual one of the rows or to columns (column 16, lines 17-39), and to compare the combined data (note, fig 9, shows the resultant image by comparing the image under voltage and image before voltage application) with a threshold (column 17, lines 6-15) to provide an indication of a malfunction in the device (fig 12, column 12, lines 56-64). Maeda is silent about a computer program to be run

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on processor. However, Hawthorne discloses a computer system including a computer program for detecting Mura defects in a substrate for a liquid crystal display program to be run on processor (column 3, lines 1-14, column 6, lines 29-48). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Maeda to include a computer program for detecting defects in a substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Maeda by the teaching of Hawthorne in which an image of the substrate previously acquired may be retrieved from computer memory using computer program, (as suggested by Hawthorne at column 9, lines 45-47).

Other prior art cited

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Guehler et al., (US.6, 221,543 B1) discloses process for making active substrates for color displays.

Hawthorne et al., (US. 5,764,209) discloses flat panel display inspection system.

Kawamura et al., (US.5, 365,034) discloses defect detection and defect removal apparatus of thin film electronic device.

Shimada (US.5, 740,272) discloses inspection apparatus of wiring board.

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Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheela C Chawan whose telephone number is 703-305-4876. The examiner can normally be reached on Monday - Thursday 8 - 6.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on 703-308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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